2023

Advanced Glass Packaging Technology™ AGPT™

FUSED SILICA AS A SUBSTRATE FOR SEMICONDUCTOR PACKAGING

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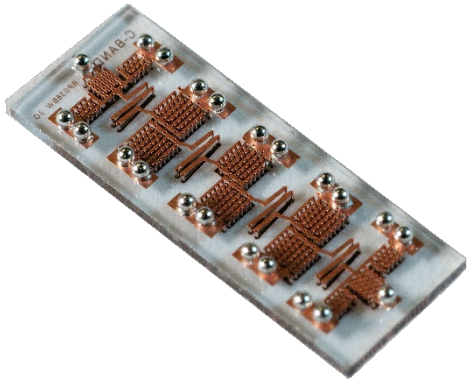
Introduction

ED2 Corporation, based in Tucson, Arizona, is comprised of a core group of scientists and Engineers with a long history in solving engineering, technology and RF challenges in a variety of contexts. As the commercial cellular industry moves to higher frequencies in search of more spectrum, the team's capability is a perfect fit for the industry.



The technical team has a long history in semiconductor packaging and is working to advance the category with fused silica, promoting a set of innovations grouped under the term "Advanced Glass Packaging Technology™ (AGPT)."

Advancements in Packaging

Semiconductor packaging is the process of designing and manufacturing packages for semiconductor devices such as microprocessors, memory chips, and other integrated circuits. These packages protect the delicate semiconductor devices and provide a way to connect them to other components in an electronic system.

There are many different types of semiconductor packages, including ball grid array (BGA), land grid array (LGA), quad flat no-lead (QFN), and plastic leaded chip carrier (PLCC). The choice of package depends on the specific requirements of the application, including the size and complexity of the device, the number of I/O (input/output) connections required, and the operating environment.

There have been several recent advancements in semiconductor packaging, including the following:

Fan-out wafer-level packaging (FOWLP): This technology allows for the creation of packages with a larger number of I/O (input/output) connections, which can improve performance and reduce the size of electronic devices.

- Embedded chip packaging: This technology involves embedding chips into a substrate, which can improve the performance and reliability of electronic devices by reducing the number of interconnections and minimizing the distance between the chip and the substrate.
- Microelectromechanical systems (MEMS) packaging: This technology involves packaging microelectromechanical systems (tiny mechanical and electromechanical devices) in a way that allows them to be integrated into electronic devices.
- Advanced packaging materials: There has been a lot of research into developing new materials for use in semiconductor packaging, such as low-k dielectric materials and advanced copper alloys, which can improve the performance and reliability of electronic devices.
- Wafer-level packaging: This technology involves packaging chips at the wafer level, which can reduce the cost and improve the performance of electronic devices by reducing the number of steps required in the packaging process.
- **3D packaging: This technology involves stacking multiple layers of chips and interconnects in a vertical configuration, which can improve performance and reduce the size of electronic devices. This is the area where ED2 Corporation is focusing its innovations.**

The Benefits of Fused silica

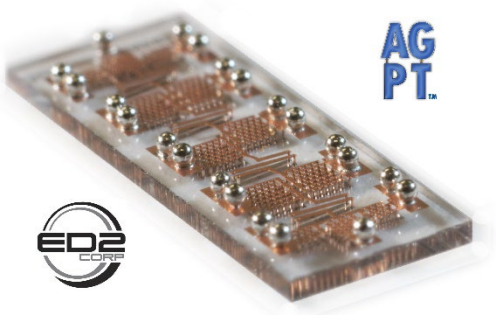
Fused silica, sometimes referred to as fused quartz, is a type of glass that is made from silicon dioxide (SiO2). It is known for its high purity, low thermal expansion, and excellent thermal shock resistance. These properties make it an ideal material for a wide range of applications, including:

1. Optics: Fused silica is used to make lenses, prisms, and other optical components because it has a very low refractive index and does not absorb UV light.
2. Semiconductor manufacturing: Fused silica is used to make components for the semiconductor industry because it is resistant to high temperatures and has a low coefficient of thermal expansion, which means it does not deform when heated.
3. Aerospace: Fused silica is used in the aerospace industry to make components that need to withstand extreme temperatures and high pressure, such as rocket nozzles and engine parts.
4. Chemical processing: Fused silica is resistant to most chemicals, making it useful in chemical processing and storage applications.
5. Medical: Fused silica is used to make medical equipment and devices, such as test tubes and pipettes, because it is chemically resistant and easy to sterilize.
6. Construction: Fused silica is used in construction because it is strong and durable, making it suitable for use in building materials, such as floor tiles and countertops.

Comparison of Organic, Silicon, and Fused Silica Substrates

Silicon, organic, and fused silica are all materials that are used as substrates in the manufacturing of electronic devices. Each type of substrate has its own unique set of properties and characteristics, which can make it suitable for different applications.

Some key differences between silicon, organic, and fused silica substrates include:



1. **Composition**: Silicon substrates are made from silicon, while organic substrates are made from materials such as polyimide and polycarbonate, and fused silica substrates are made from silicon dioxide.
2. **Thermal expansion**: Silicon and fused silica substrates have a low coefficient of thermal expansion, which means they expand and contract very little when exposed to changes in temperature. Organic substrates have a higher coefficient of thermal expansion, which means they are more prone to expansion and contraction when exposed to temperature changes.
3. **High-temperature stability**: Fused silica substrates have a high melting point and are resistant to thermal expansion, which makes them suitable for use in high-temperature environments. Silicon and organic substrates are less stable at high temperatures and may be more prone to thermal expansion and degradation.
4. **Electrical properties**: Silicon and fused silica substrates have a low dielectric constant and loss tangent, which can improve the high-frequency performance of electronic devices. Organic substrates have a higher dielectric constant and loss tangent, which can degrade the performance of high-frequency devices.

5. **Cost**: Silicon and organic substrates are generally less expensive than fused silica substrates.

Borosilicate vs Fused Silica

Borosilicate glass and fused silica are both types of inorganic, amorphous materials that are known for their high purity and excellent thermal, mechanical, and optical properties. However, there are several differences between the two materials.

Composition is one of the main differences. Borosilicate glass is made from a mixture of silica, boron oxide, and other ingredients, while fused silica is made from pure silica. As a result, borosilicate glass has a slightly different set of physical and chemical properties than fused silica.

Another difference is their thermal expansion coefficient. Fused silica has a very low thermal expansion coefficient, meaning that it expands and contracts very little when subjected to changes in temperature. Borosilicate glass has a slightly higher thermal expansion coefficient, but it is still lower than most other types of glass.

Overall, borosilicate glass and fused silica are both excellent materials for a wide range of applications, including scientific instruments, optics, and semiconductor processing. However, the specific properties of each material may make one more suitable than the other for a particular application.

Fused Silica in RF

Fused silica is an ideal material for use in RF (radio frequency) design, particularly in higher frequencies, like 5G's FR2, where it is used in a variety of applications including:

1. **Antennas**: Fused silica is used to make antennas for RF systems because it has a low dielectric constant and loss tangent, which can improve the performance of the antenna.
2. **Microwave components**: Fused silica is used to make microwave components such as waveguides and resonators because it has a low dielectric constant and loss tangent, which can improve the performance of the component.
3. **RF connectors**: Fused silica is used to make RF connectors because it is a strong and durable material that can withstand the high frequencies and power levels used in RF systems.
4. **RF packaging**: Fused silica is used in RF packaging because it has a low coefficient of thermal expansion, which helps to maintain the dimensional stability of the package and the devices within it.

Overall, fused silica is an important material in RF design because it can improve the performance and reliability of RF devices and systems by providing low loss and stable dimensions at high frequencies.

Hermetically sealed Vias with Near-Zero Topography

Fused silica components can feature filled vias, or pillars, that are effectively hermetically sealed. A hermetically sealed via with near zero surface topography is a type of via (a small conductive pathway used to connect different layers in an electronic device) that is sealed in a way that prevents the ingress of gases, liquids, or other contaminants and has a smooth, flat surface.

There are several methods that can be used to achieve a hermetically sealed via with near zero surface topography, including:

1. **High-quality sealing materials**: Vias can be sealed using materials such as glass-to-metal seals or ceramic-to-metal seals, which are designed to provide a high level of hermeticity and have a smooth, flat surface.
2. **Specialized manufacturing processes**: There are several specialized manufacturing processes, such as brazing and laser welding, that can be used to achieve a high level of hermeticity in a via and produce a smooth, flat surface.
3. **Protective coatings**: A protective coating, such as a conformal coating, can be applied to the surface of the via to provide additional protection against contaminants and smooth out any surface irregularities.

Overall, achieving a hermetically sealed via with near zero surface topography requires the use of high-quality materials and manufacturing processes to ensure that the via is sealed in a way that prevents the ingress of contaminants and has a smooth

Insulation Resistance

The insulation resistance of a substrate refers to its ability to resist the flow of electrical current through it. The insulation resistance of a substrate can be important in electronic devices because it can affect the performance and reliability of the device.

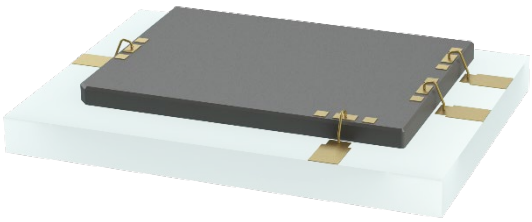
In general, silicon and fused silica substrates have a higher insulation resistance than organic substrates. This is because silicon and fused silica are non-conductive materials with a high resistance to electrical current, while organic materials are more conductive and have a lower resistance to electrical current.

However, the insulation resistance of a substrate can also be affected by other factors, such as the thickness and purity of the material, the presence of contaminants or defects, and the temperature and humidity of the environment.

Overall, the insulation resistance of a substrate is an important consideration in the design and manufacturing of electronic devices, and the choice of substrate material will depend on the specific requirements of the application.

System-in-Package Glass Modules

A system in package (SiP) glass module is a type of electronic package that integrates multiple components, such as microprocessors, memory, and other electronics, into a single module. The module is typically made from a glass substrate, which is a type of insulating material that provides mechanical support and electrical isolation for the components.



SiP glass modules have several advantages over other types of electronic packages. They allow a high level of integration and miniaturization of the electronic components, which can reduce the size and complexity of the overall system. They also provide good thermal performance, as the glass substrate has good thermal conductivity and can dissipate heat effectively. SiP glass modules are widely used in a variety of applications, including mobile devices, wearable electronics, and internet of things (IoT) devices.

Phased Array in Glass

ED2's integrated phased array in a glass module combines the phased array antenna with other electronic components, such as amplifiers, filters, and phase shifters, into a single, multi-core, glass substrate. The glass substrate provides mechanical support and electrical isolation for the components, and it can also act as a waveguide to guide the signals transmitted and received by the antenna.

Integrated phased arrays in glass modules are used in a variety of applications, including radar systems, satellite communications, and wireless telecommunications. They offer a number of advantages over traditional antennas, including the ability to transmit and receive signals over a wide range of frequencies, the ability to steer the beam of the antenna electronically, and the ability to integrate multiple antenna elements on a single substrate.

Heterogeneous Semiconductor Packaging

A heterogeneous semiconductor package combines multiple different types of semiconductor materials or technologies within a single package. This can include a combination of materials, such as silicon and compound semiconductors, or a combination of different types of semiconductor devices, such as transistors and diodes.

Heterogeneous semiconductor packages offer several benefits over traditional homogeneous packages, which are made from a single type of semiconductor material or technology. One key benefit is that they allow for the integration of multiple different functions within a single package, which reduces size and complexity of electronic systems. Heterogeneous semiconductor packages improve performance by allowing different functions to be optimized for their respective materials or technologies.

Examples of heterogeneous semiconductor packages include system-in-package (SiP) and multi-chip modules (MCM). These packages are commonly used in a wide range of electronic applications, including smartphones, computer systems, and other consumer and industrial electronics.

Benefits of Using Fused Silica in Heterogeneous Semiconductor Packaging

Fused silica can offer several benefits when used in heterogeneous semiconductor packaging:

1. **High purity**: Fused silica is made from high-purity silicon dioxide, which makes it an ideal material for use in semiconductor packaging because it can reduce contamination and improve device performance.
2. **Low coefficient of thermal expansion**: Fused silica has a low coefficient of thermal expansion, which means it does not deform or distort when exposed to temperature changes. This property can be beneficial in semiconductor packaging because it helps to maintain the integrity of the package and the devices within it, even when exposed to extreme temperatures.
3. **Excellent thermal shock resistance**: Fused silica has excellent thermal shock resistance, which means it can withstand rapid temperature changes without cracking or breaking. This makes it

suitable for use in semiconductor packaging that may be subjected to temperature cycling during use.

4. **High strength**: Fused silica is a strong and durable material, which can be beneficial in semiconductor packaging because it can help to protect the devices within the package and improve the overall reliability of the package.
5. **Chemical resistance**: Fused silica is resistant to most chemicals, which can be useful in semiconductor packaging because it can help to protect the devices within the package from exposure to chemicals during manufacturing and use.

Making and Processing Fused Silica Wafers

There are several steps involved in creating a fused silica wafer:

1. **Raw Materials**: Fused silica wafers are made from silicon dioxide, which is the primary component of sand. Other materials such as alumina, boron oxide, and silica may also be added to improve the properties of the wafer.
2. **Melting**: The raw materials are melted in a high-temperature furnace to create a glass-like substance called "frit." The frit is then poured into a mold and allowed to cool and solidify.
3. **Grinding and Lapping**: The solidified frit is then ground and lapped to create a smooth, flat surface. This process removes any surface irregularities and prepares the wafer for the next step.
4. **Polishing**: The ground and lapped wafer is then polished to a high level of finish using abrasive slurries and polishing pads. This process removes any remaining surface imperfections and creates a smooth, highly polished surface on the wafer.
5. **Inspection**: After polishing, the wafer is inspected to ensure that it meets the required specifications. Any wafers that do not meet the required specifications are rejected.
6. **Dicing**: Finally, the wafer is diced into individual wafers using a saw or laser. The wafers are then packaged and shipped to customers for use in a variety of applications.

Overall, creating a fused silica wafer requires a series of precise and carefully controlled steps to ensure the quality and consistency of the finished product.

Processing Glass: UMB/OPM

UBM (Under Bump Metallization) and OPM (On-Pad Metallization) are techniques used in the manufacturing process of glass wafers. They involve the application of a thin layer of metal, such as copper or gold, to the surface of the wafer. This metal layer is used as a bonding surface for attaching electronic components, such as transistors or integrated circuits, to the wafer. UBM is applied under the bump, while OPM is applied on the pad. Both methods are used for flip chip packaging.

Processing Glass: Wafer-to-Wafer Bonding

Wafer-to-wafer bonding is a process used to join two wafers together to form a single, larger wafer. It is used in the manufacturing of a wide range of electronic devices, including microprocessors, memory devices, and sensors.

There are several methods that can be used to achieve wafer-to-wafer bonding, including:

1. **Anodic bonding**: Anodic bonding is a process that uses high voltage and high temperature to bond two wafers together. It is typically used for bonding wafers made from materials such as silicon and glass.
2. **Thermal compression bonding**: Thermal compression bonding is a process that uses heat and pressure to bond two wafers together. It is typically used for bonding wafers made from materials such as silicon and silicon carbide.
3. **Direct bonding**: Direct bonding is a process that uses pressure and heat to bond two wafers together. It is typically used for bonding wafers made from materials such as silicon and silicon carbide.
4. **Fusion bonding**: Fusion bonding is a process that uses heat and pressure to bond two wafers together. It is typically used for bonding wafers made from materials such as silicon and silicon carbide.

Overall, wafer-to-wafer bonding is an important process in the manufacturing of electronic devices because it allows multiple wafers to be joined together to form a single, larger wafer. This can be useful for creating devices with a larger surface area or for combining multiple devices onto a single wafer.

Fused Silica Interposers

Interposers are used in electronic devices to provide a connection between different components, such as a printed circuit board (PCB) and a semiconductor chip.

Fused silica interposers offer several benefits over traditional interposers made from other materials, such as silicon or organic materials. Some of these benefits include:

1. **High-temperature stability**: Fused silica has a high melting point and is resistant to thermal expansion, which makes it suitable for use in high-temperature environments.
2. **Low coefficient of thermal expansion**: The low coefficient of thermal expansion of fused silica helps to maintain the dimensional stability of the interposer, even when it is exposed to temperature changes.
3. **High-frequency performance**: Fused silica has a low dielectric constant and loss tangent, which can improve the high-frequency performance of the interposer.
4. **Durability**: Fused silica is a strong and durable material, which can improve the overall reliability of the interposer.

Fused silica interposers are commonly used in a wide range of electronic applications, including telecommunications, aerospace, and military systems. They are also used in other high-performance applications that require stable and reliable performance, such as medical and industrial equipment.

Through Glass Vias (TGV)

Through glass vias (TGVs) are small conductive pathways that are used to connect the different layers of a printed circuit board (PCB). They are called "through glass" vias because they are formed by drilling through a layer of glass that is used as the core material in the PCB.

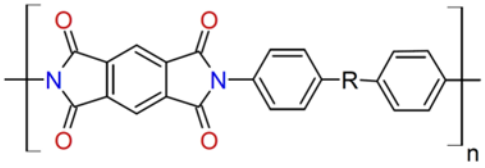
TGVs offer several benefits over traditional through-hole vias, which are formed by drilling through a layer of copper or other conductive material. Some of these benefits include:

1. **High-temperature stability**: TGVs are made from glass, which has a high melting point and is resistant to thermal expansion. This makes them suitable for use in high-temperature environments.
2. **Low coefficient of thermal expansion**: The low coefficient of thermal expansion of the glass material used in TGVs helps to maintain the dimensional stability of the PCB, even when it is exposed to temperature changes.
3. **High-frequency performance**: The glass material used in TGVs has a low dielectric constant and loss tangent, which can improve the high-frequency performance of the PCB.
4. **Durability**: The glass material used in TGVs is strong and durable, which can improve the overall reliability of the PCB.

TGVs are commonly used in devices for aerospace, and military systems. They are also used in other applications that require stable and reliable performance, such as medical and industrial equipment.

Polyimide

Polyimide is a type of polymer that is known for its excellent thermal stability, chemical resistance, and mechanical strength. It is a high-performance polymer that is used in a wide range of applications, including aerospace, electronics, and energy.



Polyimide is a thermoplastic polymer, meaning that it can be repeatedly melted and reshaped without losing its properties. It is typically made by polymerizing a precursor compound called a diamine and a dianhydride. The resulting polymer has a unique combination of properties that make it useful in high-temperature, high-performance applications.

The most known application of polyimide is as a dielectric material in electronic packaging and flexible electronic devices, it is used as a substrate for electronic devices, as a protective coating for electronic components, and as a structural material in aerospace and defense applications.

Polyimide is also used in applications such as high-temperature insulation, medical devices, and industrial machinery. It is known for its excellent resistance to high temperatures, chemicals, and radiation, which makes it useful in harsh environments.

Polyimide can be processed using different techniques such as casting, spinning, and coating. The properties of polyimide can be tailored by adjusting the composition of the polymer and the processing conditions.

Polyimide in Glass Core Modules

In a glass core module, polyimide layers are thin layers applied to the surface of the glass core to provide insulation, protection, and other desired properties.

In a glass core module, polyimide layers may be used for several purposes, including:

1. **Insulation**: Polyimide layers can be used to insulate electrical components and prevent electrical shorts.
2. **Protection**: Polyimide layers can be used to protect the glass core and other components of the module from damage due to mechanical stress, moisture, and other external factors.
3. **Adhesion**: Polyimide layers can be used to promote adhesion between different components of the module, such as the glass core and the circuit board.
4. **Other properties**: Polyimide layers can also provide other properties such as improved dimensional stability and enhanced mechanical properties.

Redistribution Layer (RDL)

A redistribution layer (RDL) is a thin film of conductive material that is used to redistribute electrical signals across the surface of a wafer. It is commonly used in the fabrication of microelectronics and other devices built on glass wafers.

RDLs are typically made of a thin film of metal, such as copper or aluminum, and are used to connect the active devices on the surface of the wafer to external electrical connections. The RDLs are typically deposited on the surface of the wafer using techniques such as physical vapor deposition (PVD) or chemical vapor deposition (CVD).

The RDLs are patterned on the wafer surface using techniques such as lithography, etching, and lift-off to create the desired electrical connections. The final RDL structure can be planar or 3D depending on the application, and it can be single or multi-layer.

Redistribution layers are crucial in modern semiconductor manufacturing, where the devices being built are becoming smaller and smaller, while the wafer thickness should remain relatively constant. RDLs are used to connect the devices to the external world and also to connect the devices to other devices on the same wafer. It also helps in reducing the parasitics and improving the performance of the devices.

Hermeticity and Fused Silica

Hermeticity refers to the ability of a device or system to be sealed in a way that prevents the ingress of gases, liquids, or other contaminants. In the context of a fused silica module, hermeticity is important because it can help to ensure the integrity and reliability of the module.

There are several ways to achieve hermeticity in a fused silica module, including:

1. **Using high-quality sealing materials**: Fused silica modules can be sealed using materials such as glass-to-metal seals or ceramic-to-metal seals, which are designed to provide a high level of hermeticity.
2. **Using vacuum packaging**: The module can be sealed in a vacuum-tight container, which can help to prevent the ingress of contaminants.
3. **Applying a protective coating**: A protective coating, such as a conformal coating, can be applied to the surface of the module to provide additional protection against contaminants.
4. **Using specialized manufacturing processes**: There are several specialized manufacturing processes, such as brazing and laser welding, that can be used to achieve a high level of hermeticity in a fused silica module.

Overall, achieving hermeticity in a fused silica module requires the use of high-quality materials and manufacturing processes to ensure that the module is sealed in a way that prevents the ingress of contaminants.

Dicing (Singulating) Glass Wafers

Dicing, or singulating, wafers involves cutting them into smaller, individual chips or die. This is typically done after the wafer has been processed and has had various devices, such as transistors or resistors, fabricated on its surface. Dicing the wafer allows the individual chips to be separated and packaged for use in electronic devices.

There are several reasons why wafers are diced. One reason is to facilitate the packaging and handling of the chips. It is much easier to work with and test individual chips than it is to handle large wafers. Dicing also allows the chips to be used in different types of packaging and to be incorporated into different types of electronic devices.

Another reason for dicing wafers is to increase the yield of the manufacturing process. If there are defects or imperfections on the wafer, dicing the wafer allows the good chips to be separated from the defective ones, increasing the overall yield of the manufacturing process.

There are several types of equipment that can be used to dice a glass wafer, including saws and lasers.

- **Saws**: A saw is a cutting tool that uses a sharp blade to cut through the material. In the case of dicing a glass wafer, a diamond-tipped saw blade is typically used. The wafer is placed on a holding fixture and the blade is used to cut the wafer into individual pieces. This process can produce wafers with relatively rough edges and may generate significant amounts of debris.
- **Lasers**: A laser is a high-energy beam of light that can be used to cut through materials. In the case of dicing a glass wafer, a laser is used to cut the wafer into individual pieces. This process is typically faster and more precise than using a saw, and it produces wafers with smooth, polished edges. However, lasers are more expensive and complex than saws, and they require special handling and safety precautions.

Overall, the choice of equipment for dicing a glass wafer will depend on the specific requirements of the application and the desired properties of the finished wafers.

De-Reballing

De-reballing refers to the removal of the existing solder balls from the surface of a packaged wafer, and the replacement of those solder balls with new ones.

The process begins with de-balling, where the old solder balls are removed from the surface of the wafer using a specialized tool or machine. This is typically done in order to repair or rework a defective package, or to repurpose the package for a different application.

Once the old solder balls have been removed, the process continues with reballing, where new solder balls are applied to the surface of the wafer. This is typically done using a machine that dispenses the new solder balls onto the surface in a precise and controlled manner. The new solder balls are then reflowed, or melted, onto the surface of the wafer to create a strong bond between the wafer and the electronic components that will be attached to it.

Laser Backside Marking

Laser backside marking is used to mark or engrave information onto the backside of a semiconductor wafer or glass substrate. This information can include things like the manufacturer's name, the date of manufacture, a serial number, or other identifying information.

The process involves using a laser to etch the information onto the backside of the wafer or substrate. The laser beam is directed onto the backside of the wafer, where it vaporizes a small portion of the material to create the desired markings. The laser beam is controlled using a computer-aided design (CAD) program, which allows for precise and accurate engraving of the information.

There are different types of laser that can be used in backside marking. The most common one is UV laser which can be used for marking on glass and semiconductor wafers. The UV laser beam is directed onto the backside of the wafer, where it vaporizes a small portion of the material to create the desired markings. It creates high contrast, high resolution and permanent marking.

This technique is widely used in the semiconductor industry, as it allows for easy identification and traceability of the wafers during the manufacturing process. Additionally, it can also be used for security and anti-counterfeiting purposes.

DryFilm

Dryfilm refers to a thin film of photoresist material that is applied to the surface of a glass wafer in a dry, or non-liquid, form. The dryfilm is then selectively exposed to light or other forms of radiation to create a pattern on the surface of the wafer. This pattern can be used as a guide for etching or other processing steps in the production of the wafer. Dryfilm photolithography is one of the key techniques used in the production of microelectronics and other devices that are built on glass wafers.

Thinning

Thinning refers to the process of reducing the thickness of a glass wafer. This is typically done in order to create thinner and/or more flexible wafers.

There are a few different methods that can be used to thin glass wafers, such as mechanical grinding and polishing, chemical etching, and laser ablation. Each of these methods has its own advantages and disadvantages, and the choice of method will depend on the desired thickness and surface finish of the final wafer, as well as the specific requirements of the application.

Thinning process is a crucial step in many semiconductor manufacturing processes, as the devices being built on the wafer are becoming smaller and smaller, while the wafer thickness should remain relatively constant, so the wafer must be thinned to maintain the same thickness.

Inking

Inking refers to the process of depositing a thin film of ink onto a wafer. This is typically done as part of a process called inkjet printing, which is used to pattern features on the wafer surface.

In inkjet printing, a wafer is coated with a thin film of photoresist material and then an ink droplets are deposited onto the surface in a precise pattern using an inkjet printer. The ink droplets act as a mask, blocking the photoresist from being exposed to light during a subsequent lithography step. The areas of the wafer that are not covered by ink will be exposed to light and then developed, creating a patterned resist layer on the wafer surface.

Inking is used for wafer fabrication for several application such as for the production of Flexible electronics, printed electronics, and also used in nano-patterning.

It is a cost-effective method of patterning a wafer, and it has the potential to enable the production of low-cost, high-volume devices on a variety of substrates, including glass, plastic, and paper.

Backmetal Evaporation

Backmetal evaporation is used to deposit a thin layer of metal onto the backside of a wafer. This is typically done to provide electrical conductivity and improve the mechanical strength of the wafer.

Backmetal evaporation is a form of physical vapor deposition (PVD) process, where a solid material is vaporized and deposited onto a substrate. In this case, the solid material is a metal, such as aluminum or copper, and the substrate is the backside of a wafer.

This process is usually done in a vacuum chamber, where a metal source (a metal rod or a metal boat) is heated to a high temperature until it evaporates, and then the metal atoms are deposited onto the wafer surface. By controlling the temperature of the source, the pressure in the chamber and the distance between the source and the wafer, the thickness and uniformity of the metal layer can be controlled.

Backmetal evaporation is used for many purposes, like providing a ground plane for the devices, improving the thermal management of the devices, and also as a barrier layer to prevent the diffusion of impurities into the substrate.

Waffle Packs

Waffle packs are a type of packaging used to protect and transport semiconductor wafers. They consist of a plastic tray with a series of wells or "cells" that hold individual wafers in place, and are typically used to transport wafers between different processing steps in a semiconductor fabrication facility.

The waffle pack is designed to hold a specific number of wafers, usually 25 or 50, and each cell is designed to hold one wafer. The wafer is placed in the cell and then covered by a lid, which is designed to protect the wafer from damage and contamination.

Waffle packs are used in wafer fabrication to protect the wafers from damage during transport and handling, and also to minimize the risk of contamination. They are often used in conjunction with

cleanroom environments, where the wafers are handled in a controlled environment to minimize the risk of contamination.

Waffle packs are also used in a variety of other applications such as in the storage of wafers and also in the shipping of wafers. They are made of materials that are compatible with the semiconductor process, like polystyrene or polypropylene, and can withstand high temperatures and chemicals.

Waffle packs have become a standard in the semiconductor industry, and they have been adopted as an industry standard for wafer handling and transportation. They are widely used in the industry and are compatible with a variety of different wafer handling equipment and automation systems.

Challenges with Semiconductor Packaging

Coefficient of Thermal Expansion (CTE) Challenges

The coefficient of thermal expansion (CTE) of a semiconductor material is a measure of how much the material expands or contracts when exposed to changes in temperature. In semiconductor applications, the CTE of the materials used can be a significant challenge because mismatches in CTE between different materials can lead to problems such as stress and strain, which can damage or degrade the performance of the device.

$$\frac{\Delta L}{L} = \alpha[\Delta T]$$

ΔL = change in Length
ΔT = change in Temperature
α = Coefficient of Thermal Expansion (CTE)

Some of the challenges associated with the CTE of semiconductor materials include:

1. **Thermal expansion mismatch**: Different semiconductor materials can have significantly different CTEs, which can cause problems when they are used in the same device or system. For example, if a device has components made from materials with different CTEs, the components may expand or contract at different rates when the device is exposed to temperature changes, which can cause stress and strain within the device.
2. **Reliability issues**: Mismatches in CTE can also lead to reliability issues in semiconductor devices, such as cracking or breakage due to thermal stresses.
3. **Performance degradation**: The CTE of a semiconductor material can also affect its electrical and mechanical properties, which can lead to degradation in device performance over time.

To mitigate these challenges, semiconductor manufacturers often use materials with similar CTEs and design devices to minimize the impact of thermal expansion mismatches. They may also use techniques such as stress relief annealing to reduce the impact of thermal stresses on the device. ED2 has substantial industry knowledge and trade secrets around the art of mitigating CTE mismatch issues.

Thermal Optimization

Thermal optimization of silicon devices is important for several reasons. Silicon is a widely used material in the electronics industry because of its high electrical conductivity and relatively low cost. However, it

is also a good thermal conductor, which means that it can generate a lot of heat when it is used in high-power devices such as processors or power amplifiers.

If the heat generated by a silicon device is not properly managed, it can lead to a number of problems. As one example, excessive heat can cause a device to fail or malfunction, and it can also reduce the device's lifespan. In addition, heat can cause the device to consume more power, which can reduce its efficiency.

To optimize the thermal performance of silicon devices, ED2's engineers employ a variety of techniques. These include designing the device to minimize the amount of heat generated, using materials with good thermal conductivity to dissipate heat more effectively, and implementing active cooling solutions such as fans or heat sinks. By optimizing the thermal performance of silicon devices, we can improve their reliability, lifespan, and efficiency.

Thermal optimization with copper and fused silica can be achieved through a variety of methods, including:

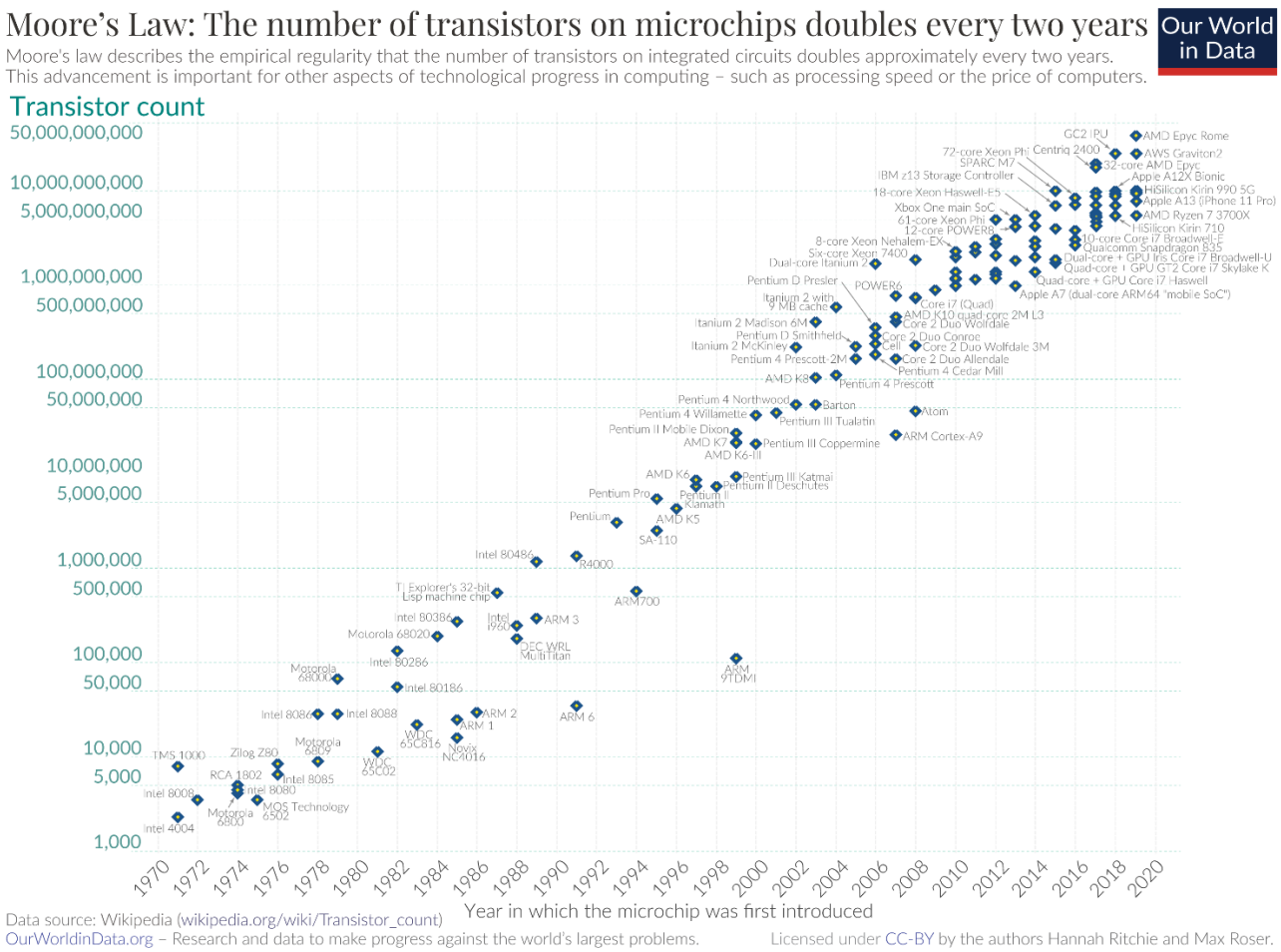
1. **Using copper and fused silica materials with similar coefficients of thermal expansion (CTE)**: Mismatches in CTE can cause stress and strain in a device, leading to performance degradation and reliability issues. By using materials with similar CTEs, it is possible to minimize the impact of thermal expansion on the device.
2. **Designing devices to minimize the impact of thermal expansion**: This can include using structures such as strain reliefs or support beams to distribute thermal stresses evenly throughout the device.
3. **Using thermal management techniques**: Techniques such as heat sinking, thermal vias, and thermal paste can help to dissipate heat from the device and reduce the impact of thermal expansion on the device.
4. **Applying stress relief annealing**: This is a process that involves heating a device to a high temperature and then slowly cooling it to relieve thermal stresses. This can help to reduce the impact of thermal expansion on the device and improve its reliability.

By using these methods, it is possible to optimize the thermal performance of devices that use copper and fused silica materials and improve their reliability and performance.

Challenges with Fan Out Packaging

Fan-out in semiconductor packaging refers to the process of distributing the input/output (I/O) connections of a chip to the perimeter of the package. This allows for a smaller package size and better performance, but it can also introduce several challenges and issues.

One issue with fan-out packaging is the difficulty of creating ultra-small and precise features on the scale of nanometers. As feature sizes continue to shrink, it becomes increasingly difficult to control the properties of the materials being used, which can lead to defects and variability in the finished product. This can be particularly challenging in fan-out packaging, where the I/O connections must be distributed over a large area and must be highly reliable.



Another issue with fan-out packaging is the cost and complexity of the equipment needed to manufacture these packages. Fan-out packaging requires advanced and expensive equipment such as wafer-level packaging machines and advanced lithography systems, which can increase the cost of production.

In addition, fan-out packaging requires advanced process control and monitoring techniques to ensure the quality of the finished product. This can be particularly challenging in a manufacturing environment, where there are many variables that can affect the performance of the package.

Overall, fan-out packaging has many benefits, but it also introduces several challenges and issues that must be carefully considered in order to ensure the reliability and performance of the finished product.

Drilling Fused silica

Drilling fused silica can be challenging due to the material's high hardness, low thermal conductivity, and tendency to produce a large amount of abrasive dust when being machined. Some specific challenges that may be encountered when drilling fused silica include:

- **Tool wear**: Fused silica is a very hard material and can cause rapid wear on drill bits and other cutting tools. This can result in shortened tool life and increased tooling costs.

- **Heat generation**: Fused silica has low thermal conductivity, which means it does not dissipate heat well. This can lead to high temperatures being generated at the cutting edge, which can cause tool failure and material damage.
- **Abrasive dust**: Fused silica produces a large amount of abrasive dust when being machined, which can cause respiratory issues for workers and can also clog and damage cutting tools.
- **Chip control**: Fused silica has a tendency to produce long, stringy chips when being drilled, which can cause problems with chip evacuation and can lead to tool failure.
- **Surface finish**: Fused silica can be difficult to machine to a high degree of surface finish, as it tends to produce a rough finish when being machined.

Metallization

Metallization of fused silica presents several challenges:

- **Adhesion**: Fused silica has a very smooth, non-porous surface, which can make it difficult for metal to adhere to it. This can be overcome by using specialized adhesion promoters or by roughing up the surface of the fused silica prior to metallization.
- **Surface roughness**: Fused silica has a tendency to produce a rough surface finish when being machined, which can make it difficult to achieve a smooth, uniform metal coating.
- **Contamination**: Fused silica is a very pure material and is prone to contamination by foreign particles. Care must be taken to prevent contamination during the metallization process to ensure high quality coatings.
- **Process control**: Metallization of fused silica requires precise process control in order to achieve the desired results. This can be challenging due to the sensitivity of the materials and processes involved.
- **Cost**: Metallization of fused silica can be a costly process due to the specialized equipment and materials required.

Polishing Fused silica

Polishing fused silica can be a challenging process due to its hardness and transparency. Here are a few tips for polishing fused silica:

1. Start with a coarse grit diamond abrasive and gradually work your way up to finer grits.
2. Use a slurry of abrasive and water to facilitate the polishing process.
3. Use a soft, compliant pad to apply pressure to the surface being polished.
4. Keep the surface cool by regularly rinsing it with water or using a cooling fluid.
5. Use a polishing compound to achieve a high-quality finish.
6. Inspect the surface regularly to ensure that it is evenly polished.

It is important to use caution when polishing fused silica, as it is brittle and can break if handled improperly. Proper handling and use of the correct tools and techniques can help ensure a successful polishing process.

Solder Balls

Adding solder balls to fused silica can be challenging due to the differences in the physical and chemical properties of the two materials. Here are a few challenges that may arise when adding solder balls to fused silica:

- **Adhesion**: It can be difficult to get the solder balls to adhere to the surface of the fused silica due to the differences in their physical and chemical properties.
- **Surface roughness**: The surface of fused silica is usually very smooth, which can make it difficult for the solder balls to adhere to the surface.
- **Contamination**: Fused silica is highly resistant to chemical attack, but the fluxes and other materials used in the soldering process can be corrosive. If they come into contact with the fused silica, they can cause contamination and affect the quality of the final product.

To overcome these challenges, it is important to carefully clean and prepare the surface of the fused silica before soldering, use the correct soldering materials and conditions, and carefully control the soldering process to ensure a uniform and high-quality finish.

Dicing and Singulation

Dicing and singulation of fused silica can be challenging due to the material's high hardness and transparency. Fused silica is a high-purity, transparent glass-like material made from silicon dioxide. It is extremely hard and has a very low coefficient of thermal expansion, which means it does not expand or contract significantly when subjected to temperature changes.

Here are a few challenges dicing and singulating fused silica:

- **Fracture**: Fused silica is brittle and can easily break or shatter if it is not handled carefully.
- **Edge quality**: The edges of the fused silica wafers can be prone to chipping or roughness if they are not cut cleanly.
- **Contamination**: Fused silica is highly resistant to chemical attack, but the abrasive materials and coolants used in the dicing process can potentially contaminate the surface of the wafers.

To overcome these challenges, it is important to use the correct tools and techniques for dicing and singulating fused silica. This may include using specialized saw blades or laser systems, carefully controlling the cutting conditions, and using clean and uncontaminated materials and coolants. It is also important to handle the wafers carefully to avoid damaging them.

Inspection and Test

Inspecting and testing heterogeneous modules made from fused silica can be challenging due to the complexity of the systems and the various materials and components that they are made of. Here are a few tips for inspecting and testing heterogeneous modules:

- Develop a clear understanding of the module's design and intended use. This will help you identify the key components and functions that need to be tested and inspected.
- Use a variety of inspection and testing methods to ensure that all aspects of the module are thoroughly evaluated. This may include visual inspection, dimensional measurement, functional testing, and destructive testing.
- Consider the impact of different environments and operating conditions on the module's performance. Test the module under a range of conditions to ensure that it can withstand the stresses it will encounter in its intended use.
- Use specialized equipment and techniques as needed to test and inspect specific components or materials. For example, you may need to use microscopes, X-ray equipment, or specialized testing fixtures to evaluate small or complex components.

- Keep accurate records of your inspection and testing results, including any issues or defects that are identified. This will help you track the performance of the module over time and identify areas for improvement.

Conclusion

Fused silica offers a number of advantages as a substrate for semiconductor packaging and for the creation of high-frequency RF devices. When engaged in the project of developing a device in fused silica, it's important to understand all of the operations involved, and best practices around ensuring a successful implementation.

ED2 CORPORATION is always ready to help and or support these initiatives with an extensive collection of technologies, innovations, and experienced team members.

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