Coefficient of Thermal Expansion (CTE) and Fused Silica

CTE

The coefficient of thermal expansion (CTE) is a measure of how much a material expands or contracts when its temperature changes. This paper assumes the reader is already familiar with the basic principles of thermal expansion.

Different materials have different coefficients of thermal expansion, and these values are usually provided by manufacturers or can be found in material properties databases. CTE is an essential property to consider in engineering and construction, as it can have significant implications for the behavior and performance of materials under temperature variations, especially in applications where thermal stability is critical.

When two connected materials have different CTE values, that is called “CTE mismatch.” CTE mismatch can create several problems in space applications, especially in the construction and operation of satellites, spacecraft, and other space-based systems.

- **Thermal Stress and Fatigue**: In space, objects experience extreme temperature variations, from extreme cold in the shadow to intense heat when exposed to the sun. Different materials used in the construction of spacecraft can have different coefficients of thermal expansion. Over time, this stress can cause structural degradation and potential failures.

- **Distortion and Misalignment**: CTE mismatch can cause parts of a space structure to distort or become misaligned as they experience temperature fluctuations. This misalignment can affect the performance and functionality of sensitive components, such as optics, solar panels, and antennas.

- **Thermal Cycling Issues**: Repeated thermal cycling can exacerbate CTE mismatch problems. Thermal cycling can induce fatigue and cause parts to weaken, leading to mechanical failures and decreased reliability.

- **Joint and Interface Problems**: When different materials with different CTE values are bonded or joined together, CTE mismatch can cause stress concentrations at the interfaces. This can lead to cracking or delamination at the joint, compromising the structural integrity.

- **Sensor and Instrument Accuracy**: In precision instruments and sensors, variations in temperature can cause components to expand or contract, leading to shifts in the instrument's calibration and measurement accuracy.

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- **Deployment and Mechanism Issues**: In space missions that involve deploying components like solar panels, booms, or antennas, CTE mismatch can affect the smooth operation of these mechanisms. Misalignments or binding can prevent proper deployment or retraction.

CTE mismatch can be mitigated and managed in various ways. Here are some of the best ways to manage CTE mismatch:

- **Material Selection**: Careful selection of materials with compatible CTE values can be very helpful. Using materials with similar CTEs helps minimize the stress generated by temperature variations. It is crucial to consider CTEs not only for the base materials but also for adhesives, solders, and other joining materials used in the assembly. Options such as low CTE ceramics, composites, or specialized alloys can be considered for specific applications. The CTE of high purity fused silica is around 0.55 x 10^-6 /°C (microstrain/°C) over a temperature range of 0°C to 200°C.

  Using heavier copper weights in the PCB design can help with heat dissipation. Thicker copper layers provide better thermal conductivity and can help to reduce the temperature gradients across the board.

- **Design and Layout Optimization**: Distributing and balancing thermal stresses across the structure can reduce localized stress concentration. Techniques like using serpentine routing for traces, introducing slotted vias, or incorporating flexible joints can help accommodate thermal expansion or contraction without excessive stress build-up.

  If your design requires controlled impedance traces, use materials with closely matched CTE values for the signal layers. This helps to maintain the desired impedance characteristics over temperature variations.

  For components with large ground or power pads, it's suggested to use thermal relief pads instead of solid copper planes. Thermal relief pads have narrower connections to the copper planes, allowing for better expansion and contraction during temperature changes.

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- **Thermal Management**: By maintaining more uniform temperatures across the system, thermal gradients and associated stresses can be minimized. This can be achieved, for example, by using heat sinks, heat spreaders, thermal insulation, or active cooling systems.

  A 2020 article in Nature describes how microfluidics can be used with extreme efficiency in the cooling of electronics, both further enabling miniaturization of electronics and reducing energy consumption. (van Erp, 2020) Fused silica is a perfect material to use for microfluidics.

  An Aluminum Diamond heat sink (heat spreader) can be incorporated into the package in the form of a flange. The table below shows a comparison of different materials that can be used as heat spreaders.

Material	Structure	Thermal Conductivity (W/mK)	CTE (ppm/K)
Cu	Pure	393	17
Diamond		1500	1.4
Silicon		136	4.1
SiC	4H-Si	430	4
AlSic	63% SiC	>175	7.9
W90Cu	90% W	185	6.5
W75Cu	75% W	225	9
Mo70Cu	70% Mo	185	9.1
Mo50Cu	50% Mo	250	11.5
CuMoCu	1:4:1	220	6
CuMoCu	1:1:1	310	8.8
Cu/Mo70Cu/Cu	1:4:1 laminate	340	8

Figure 1. GaN HEMT Technical Status: Transistors and MMICs for Military and Commercial Systems. Ray Pengelly, Cree RF, Research Triangle. Paper at IMS 2009 Boston; Provided by NanoMaterials Int. Corp.

  Below is an example of heat spreader that can be incorporated into the glass package.

Figure 2. Heat spreader

- **Design for Reliability**: Designing for reliability involves considering factors such as fatigue life, creep, and stress relaxation. Understanding the expected thermal cycling and stress levels that the materials and components will experience over the mission's lifetime is crucial. Applying appropriate safety factors, conducting accelerated life testing, and ensuring adequate margins can help improve the long-term reliability of the system.

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- **Mechanical Stress Relief**: Incorporating stress relief mechanisms into the design can help alleviate the effects of CTE mismatch. These mechanisms may include compliant layers, flexible interconnects, or intentionally introduced stress relief features. These features can absorb or redistribute stress caused by differential thermal expansion, reducing the potential for failures or damage.

- **Simulation and Testing**: Thorough simulation and testing are essential to verify the performance and reliability of the system under different thermal cycling scenarios. Finite element analysis (FEA) can be used to simulate and predict the response to thermal stresses. Additionally, conducting environmental testing, including thermal cycling tests, can help validate the design and identify potential failure points.

- **Packaging Techniques**: Choosing appropriate packaging techniques can also aid in managing CTE mismatch. Wafer-level packaging or chip-scale packaging approaches can help reduce CTE-related stresses by integrating components closer to the substrate or package material. Additionally, the use of compliant or flexible interconnects, such as elastomer-based connectors, can provide some degree of stress relief.

  In traditional packaging methods, the integrated circuit (IC) die is mounted on a separate package substrate, and wire bonds or solder balls are used for interconnections. These interconnections can have different CTE values from the IC die and the substrate, leading to CTE mismatch. In wafer-level packaging, as with fused silica, the interconnections are directly built on the wafer before dicing, resulting in shorter interconnection lengths. Shorter interconnections help minimize mechanical stress caused by CTE mismatch.

- **Compliance with Industry Standards**: Following industry standards and guidelines specific to space applications can help ensure proper CTE management. Organizations such as the European Cooperation for Space Standardization (ECSS) and the National Aeronautics and Space Administration (NASA) provide standards and best practices for space-grade electronic components and systems.

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Comparing CTE of Fused Silica to Other Substrates

Fused silica has a low CTE compared to many other substrate materials. In fact, fused silica has one of the lowest CTE values of any commonly used substrate material.

For comparison, here are some typical CTE values for various substrate materials:

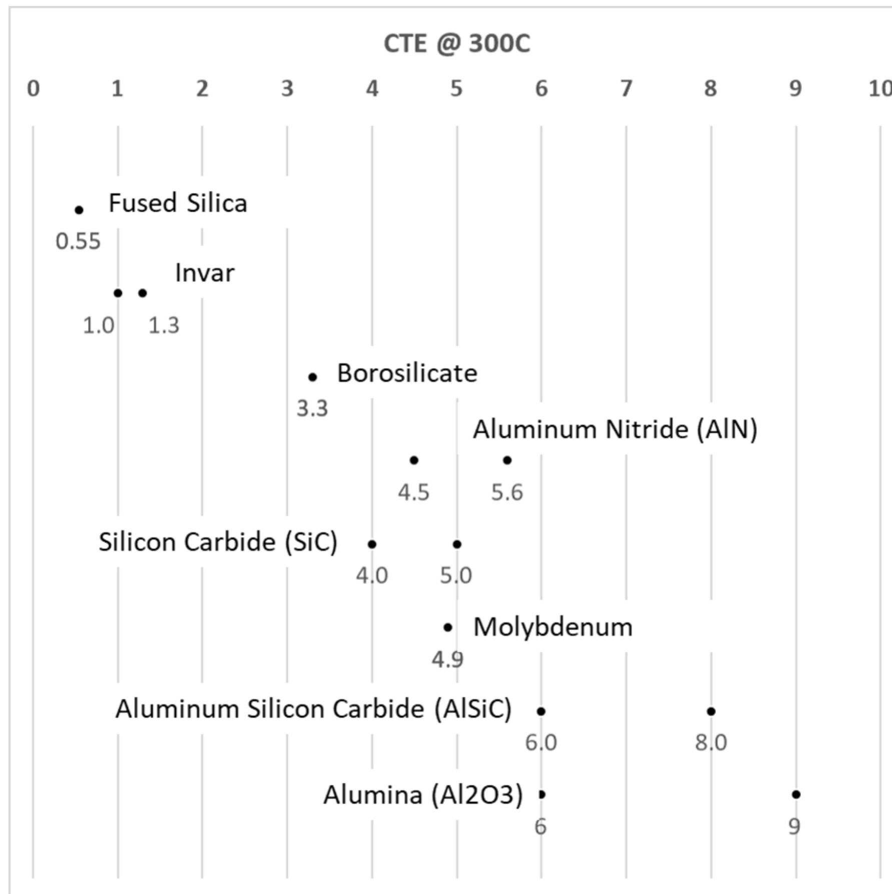

Figure 3. CTE Values for Various Substrates

Substrate	Min	Max
Fused Silica	0.55	0.55
Invar	1.0	1.3
Borosilicate	3.3	3.3
Aluminum Nitride (AlN)	4.5	5.6
Silicon Carbide (SiC)	4.0	5.0
Molybdenum	4.9	4.9
Aluminum Silicon Carbide (AlSiC)	6.0	8.0
Alumina (Al2O3)	6	9

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With a much lower CTE than most other commonly used substrate materials, fused silica can make it a good choice for applications where dimensional stability is important, such as in optics, MEMS devices, and other precision instruments.

Overall, the choice of substrate material depends on the specific requirements of the application, and a number of factors should be considered beyond just the CTE, such as the mechanical strength, thermal conductivity, and other properties of the material.

Solder Balls and CTE

ED2 has mastered the use of solder balls with fused silica for thermal management and mitigation of CTE mismatch. Solder balls compensate for CTE mismatch by acting as compliant interconnections.

When exposed to temperature changes, solder balls can deform and absorb the mechanical stress caused by CTE mismatch. This flexibility allows the solder balls to accommodate the differential expansion and contraction of the materials, reducing the strain on the components.

Solder balls also provide thermal stress relief by acting as a buffer between the component and the substrate or PCB. As the assembly experiences temperature variations, solder balls undergo elastic deformation, absorbing thermal expansion mismatch and preventing excessive stress from being transmitted to the component or the board.

With the correct alloy selection, like lead-free SAC (SnAgCu), solder balls offer good thermal conductivity. This allows them to efficiently transfer heat generated by the component to the PCB or substrate.

Thermal Modeling with Fused Silica

Thermal modeling in a circuit assembly involves analyzing and predicting the temperature distribution and heat flow within the components and overall system. It helps in understanding and optimizing the thermal behavior of the circuit assembly to ensure reliable operation and prevent thermal-related failures.

- **Component Characterization**: The first step is to gather information about the components in the circuit assembly, such as power dissipation, thermal resistance, and thermal capacitance.

- **Geometry Creation**: The circuit assembly's physical layout and geometry can then be represented in the thermal modeling software, or in calculations. 3D modeling involves creating a 3D model or a simplified 2D representation of the assembly, including all the components, printed circuit boards (PCBs), heat sinks, enclosures, and any other relevant structures.

- **Material Properties**: Each material in the assembly, such as the PCB, solder, and thermal interface materials, is assigned specific thermal properties, including thermal conductivity, specific heat, and density. These properties influence how heat is transferred through the materials.

- **Boundary Conditions**: Boundary conditions are defined to simulate the thermal environment in which the circuit assembly operates. This includes setting ambient temperature, specifying heat

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sources or sinks, and considering any external cooling mechanisms like fans or heat exchangers.

Heat Transfer Simulation: Thermal modeling software solves a set of mathematical equations based on principles of heat transfer, such as conduction, convection, and radiation.

- **Iterative Analysis**: Thermal modeling software can iteratively calculate the temperature distribution within the circuit assembly, based on the initial conditions, boundary conditions, and material properties, taking into account factors such as power dissipation of components, thermal resistances between components and their surroundings, and the heat transfer paths within the assembly.

- **Result Analysis**: Once the simulation converges, the thermal modeling software provides visual representations of the temperature distribution, heat flow paths, and potential hotspots within the circuit assembly. This information helps identify areas that might experience excessive heating and can guide design modifications or thermal management strategies.

- **Optimization and Validation**: The thermal model can be used to optimize the circuit assembly design by experimenting with different materials, component placement, heat sink configurations, and cooling mechanisms. The model can also be validated by comparing its predictions with actual temperature measurements obtained from prototypes or testing.

A Sample Thermal Model with Fused Silica

ED2 Corporation is using fused silica in a variety of designs. Thermal models have been generated to ensure that maximum specified temperatures are not exceeded, and to facilitate best design implementations. Below is summary data taken from the thermal analysis.

The die part used in this model is the Microchip ICP1747. It's a 50W GaN PA MMIC. The specification indicates a maximum junction temperature of 275°C. ED2 packaged the part in two layers, with the bottom core being fused silica, upon which the die is epoxied, as shown below.

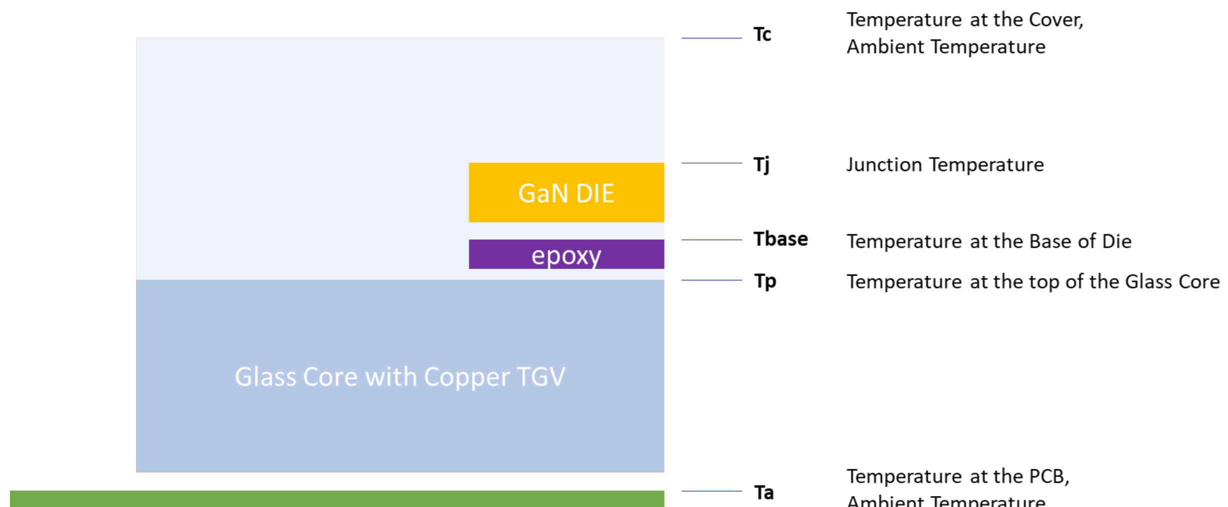

Figure 4. Thermal Model Overview

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Assumptions

The following assumptions were made for the purposes of modeling this package.

1. Substrate is high-purity fused silica
2. Glass area = Microchip die area = epoxy area (4.5 mm x 6.5 mm)
3. Appli-Tec 5200 epoxy thermal conductivity = 2.5 W/mK, thickness of epoxy = 0.001”
4. Die thermal resistance is 1 C/W
5. Assumed 5 Amp (spec is TBD)

The packaged die is rated at 50W output power (Pout). With an ambient temperature of 85C, the glass package shown above can easily dissipate power to keep the junction temperatures well below the rated maximum value of 275C.

Figure 5.Thermal Model

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ED2 and Advanced Glass Packaging Technology AGPT™

ED2 Corporation has developed a technology platform called Advanced Glass Packaging Technology (AGPT™) upon which it is creating a variety of products.

- **Passive Components**. These components can be interposer, RF passives, or simply an interconnect. ED2 has a variety of bandpass filters developed in fused silica. From lumped element at Sub-6Ghz to waveguides at high frequency (39 GHz). At wafer scale, parts can be produced with high yield and low cost all the way up to over 100GHz.

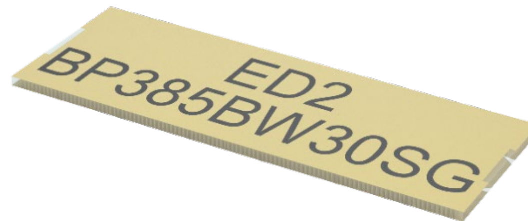

Figure 6. Fused Silica Waveguide Filter

- **Glass Packaging.** ED2 is developing a platform called Advanced Glass Packaging Technology™ (AGPT). This platform is performant up to 100 GHz and is being used to create both custom and OEM products.

Figure 7. Mixer Module in Glass

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ED2 is able to package higher density DIE chips and fan out in a multi-layered configuration and embed passive components.

The packaging supports small feature sizes for widths and gaps much better than organic or ceramic-based materials. Line spacing and trace widths can be as small as 10-20µm.

ED2 creates multi-core glass modules integrating both copper-filled vias and redistribution layers (RDL) making electrical and RF connections in and out of the chips, essentially producing 3D circuits. The package can incorporate a heatsink in the form of a flange or a heatsink mechanism to spread and dissipate heat, as needed. Using Aluminum Diamond as a heat sink, heat can be dissipated with great efficiency, and is lightweight reliable, with a matched CTE to silicon and fused silica.

ED2 Corporation

ED2 is comprised of a core group of Scientists and Engineers with a long history in the aerospace, defense, and wireless telecom. The ED2 team came together in 2018 and has been innovating around both custom and OEM components, subassemblies, and products.

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